UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/821,163 | 03/28/2001 | Toshiyuki Kouchi | 2102475-991110 | 4019 |

26379 7590 07/26/2004

GRAY CARY WARE & FREIDENRICH LLP
2000 UNIVERSITY AVENUE
E. PALO ALTO, CA 94303-2248

| EXAMINER | |
|---|---|
| DOOLEY, MATTHEW C | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2133 | 7 |

DATE MAILED: 07/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/821,163 | KOUCHI ET AL. | |
| | Examiner | Art Unit | |
| | Matthew C. Dooley | 2133 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *27 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☒ Claim(s) *19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04/27/04* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Allowable Subject Matter*

1. As cited in the previous office action, mailed 01/29/04, claim 19 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record fails to teach to the limitations of claim 19 and as such, claim 19 contains allowable subject matter and would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### *Response to Arguments*

2. Applicant's arguments, see paper 5, filed 04/27/04, with respect to 9-18 have been fully considered and are persuasive, and as such have been withdrawn. The amendment of claims 1-8 necessitate new grounds of rejection. The rejection of claims 1-18 are listed below.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 9-14, 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Won et al., U.S. 6,216,240.

As per claim 9:

Won teaches to a plurality of DRAM circuits (Fig.1: 17,19), a plurality of control circuits corresponding to a specified RAM circuit, that receive a test control signal to perform a test control in which the RAM circuits are tested (Fig.2: 25; Fig.3: 35a,35b), and an output selector that is controlled by a control circuit signal and outputs signals of the DRAM circuitry at the time of the test to an output terminal (Fig.4: 47).

As per claim 10:

The control circuitry of Won is directly connected to a control signal input terminal and is controlled by said control signal input terminal (Fig.2: 25; Fig.3: 35).

As per claim 11:

The circuitry of Won further incorporates an input terminal selector for receiving a DRAM macro signal (Fig.2: 23; Fig.3: 33).

As per claim 12:

The control circuitry of Won is directly connected to a control signal input terminal and is controlled by said control signal input terminal (Fig.2: 23,25; Fig.3: 33,35).

As per claim 13:

The system of Won teaches to an output selector that is controlled by the control circuit that outputs a DRAM macro signal from one of the DRAM circuits during normal operation (Fig.4: 47).

As per claim 14:

The control circuitry of Won is directly connected to a control signal input terminal and is controlled by said control signal input terminal (Fig.2: 23,25; Fig.3: 33,35; Fig.4: 43,45).

As per claim 17:

Won teaches to a plurality of DRAM circuits (Fig.1: 17,19), a control circuitry that receive a test control signal and controls the DRAM circuitry simultaneously and independently (Fig.3: 35), an input selector that inputs a DRAM macro signal to one of the DRAM circuits (Fig.2: 23; Fig.3: 33), and an output selector that outputs signals of the DRAM circuitry at the time of the test to an output terminal (Fig.4: 47).

***Claim Rejections - 35 USC § 103***

5. Claims 1-8, 15-16, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Won et al., U.S. 6,216,240, in view of Duesman, U.S 6,169,695, and the applicant's admitted prior art (APA: Fig.7-9; Specification: Pg.2:1 – Pg.5:1).

As per claim 1:

Won teaches to a plurality of DRAM circuits (Fig.1: 17,19), a control circuit that receives a test control signal to perform a test control in which the RAM circuits are tested (Fig.2: 23; Fig.3: 33), an input selector that is controlled by the control circuit and inputs a DRAM macro signal to the DRAM circuitry at the time of the test (Fig.2: 25; Fig.3: 35), and an output selector that is controlled by the control circuit and outputs signals of the DRAM circuitry at the time of the test (Fig.4: 47). However, not clearly taught by Won is the methodology of testing the DRAM circuits. The APA teaches to DRAM circuitry while the access of the DRAM circuitry is changed for each row for

cyclically accessed DRAM circuitry for both a single DRAM followed by a secondary DRAM, as well as a row of a first DRAM followed by a row of a second DRAM, then onto a second row of the first DRAM, and to a second row of the second DRAM and so forth in a cyclically accessed manner (APA: Fig.7-9). It would have been obvious for one of ordinary skill in the art at the time of the invention to make use of the testing methodology taught by the APA in conjunction with the testing circuitry of Won because the implementation of the teachings of the APA allow for a specific testing methodology for multiple DRAM circuitry (APA: Specification: Pg.4:15 - Pg.5:1).

As per claim 2:

The control circuit of Won is directly connected to a control signal input terminal and is controlled by said control signal input terminal (Fig.2: 23; Fig.3: 33).

As per claim 3:

The system of Won teaches to an input selector that is controlled by the control circuit inputs a DRAM macro signal to one of the DRAM circuits during normal operation (Fig.3: 35).

As per claim 4:

The control circuit of Won is directly connected to a control signal input terminal and is controlled by said control signal input terminal (Fig.2: 23; Fig.3: 33).

As per claim 5:

The system of Won teaches to an output selector that is controlled by the control circuit that outputs a DRAM macro signal from one of the DRAM circuits during normal operation (Fig.4: 47).

As per claim 6:

The control circuit of Won is directly connected to a control signal input terminal and is controlled by said control signal input terminal (Fig.2: 23,25; Fig.3: 33,35).

As per claim 7:

The APA teaches to accessing the first rows of the DRAM circuits while changing the access to the DRAM circuits, and following the access to the first rows, the access is performed to the next rows through the last rows of the DRAM circuits while changing the access to the DRAM circuits (Fig.7-9).

As per claim 8:

The control circuit of Won is directly connected to a control signal input terminal and is controlled by said control signal input terminal (Fig.2: 23,25; Fig.3: 33,35).

As per claim 15:

Won teaches to the limitations of claim 9, as illustrated in the rejection of claim 9 above. Claim 15 depends directly on claim 9. The remaining limitations of claim 15 are taught by the APA whereby the first rows of the DRAM circuits while changing the access to the DRAM circuits, and following the access to the first rows, the access is performed to the next rows through the last rows of the DRAM circuits while changing the access to the DRAM circuits (APA: Fig.7-9). The combination of Won and the APA is shown above with respect to claim 1 and is further applied in the rejection of claim 15.

As per claim 16:

The control circuitry of Won is directly connected to a control signal input terminal and is controlled by said control signal input terminal (Fig.2: 23,25; Fig.3: 33,35).

As per claim 18:

Won teaches to the limitations of claim 17, as illustrated in the rejection of claim 17 above. Claim 18 depends directly on claim 17. The remaining limitations of claim 17 are taught by the APA whereby the DRAM circuits are accessed sequentially and the information is transferred to outside the dram circuitry (APA: Fig.7-9). The combination of Won and the APA is shown above with respect to claim 1 and is further applied in the rejection of claim 18.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Dooley whose telephone number is (703) 306-5538. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew Dooley
Examiner AU 2133
07/15/04

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100